

FIG. 1 is a block diagram of a system 20 according to one embodiment of the present invention. The system 20 includes a processor 22, a memory controller 31, and a memory 26. The memory controller 31 is connected to the processor 22 via a bus 29. The memory controller 31 is also connected to the memory 26 via a bus 28. The memory 26 includes a plurality of memory cells 30, each of which is connected to a word line 32 and a bit line 38. The memory controller 31 is configured to control the memory cells 30 via the word lines 32 and the bit lines 38. The memory controller 31 includes a control logic 34 and a control signal generator 36. The control logic 34 is configured to generate control signals for the memory cells 30 via the control signal generator 36. The control signal generator 36 is configured to generate control signals for the memory cells 30 via the word lines 32 and the bit lines 38. The memory controller 31 is also connected to the memory 26 via a data bus 30. The memory 26 is configured to store data received from the processor 22 via the data bus 30 and to provide data to the processor 22 via the data bus 30. The memory 26 is also connected to the memory controller 31 via a control bus 32. The memory controller 31 is configured to control the memory 26 via the control bus 32. The memory controller 31 is also connected to the memory 26 via a power supply 38. The power supply 38 is configured to provide power to the memory cells 30 via the word lines 32 and the bit lines 38. The memory controller 31 is also connected to the memory 26 via a ground 38. The ground 38 is configured to provide a common reference potential for the memory cells 30 via the word lines 32 and the bit lines 38. The memory controller 31 is also connected to the memory 26 via a clock signal 38. The clock signal 38 is configured to provide a clock signal to the memory cells 30 via the word lines 32 and the bit lines 38. The memory controller 31 is also connected to the memory 26 via a data signal 38. The data signal 38 is configured to provide a data signal to the memory cells 30 via the word lines 32 and the bit lines 38. The memory controller 31 is also connected to the memory 26 via a control signal 38. The control signal 38 is configured to provide a control signal to the memory cells 30 via the word lines 32 and the bit lines 38. The memory controller 31 is also connected to the memory 26 via a power supply 38. The power supply 38 is configured to provide power to the memory cells 30 via the word lines 32 and the bit lines 38. The memory controller 31 is also connected to the memory 26 via a ground 38. The ground 38 is configured to provide a common reference potential for the memory cells 30 via the word lines 32 and the bit lines 38. The memory controller 31 is also connected to the memory 26 via a clock signal 38. The clock signal 38 is configured to provide a clock signal to the memory cells 30 via the word lines 32 and the bit lines 38. The memory controller 31 is also connected to the memory 26 via a data signal 38. The data signal 38 is configured to provide a data signal to the memory cells 30 via the word lines 32 and the bit lines 38. The memory controller 31 is also connected to the memory 26 via a control signal 38. The control signal 38 is configured to provide a control signal to the memory cells 30 via the word lines 32 and the bit lines 38.

20

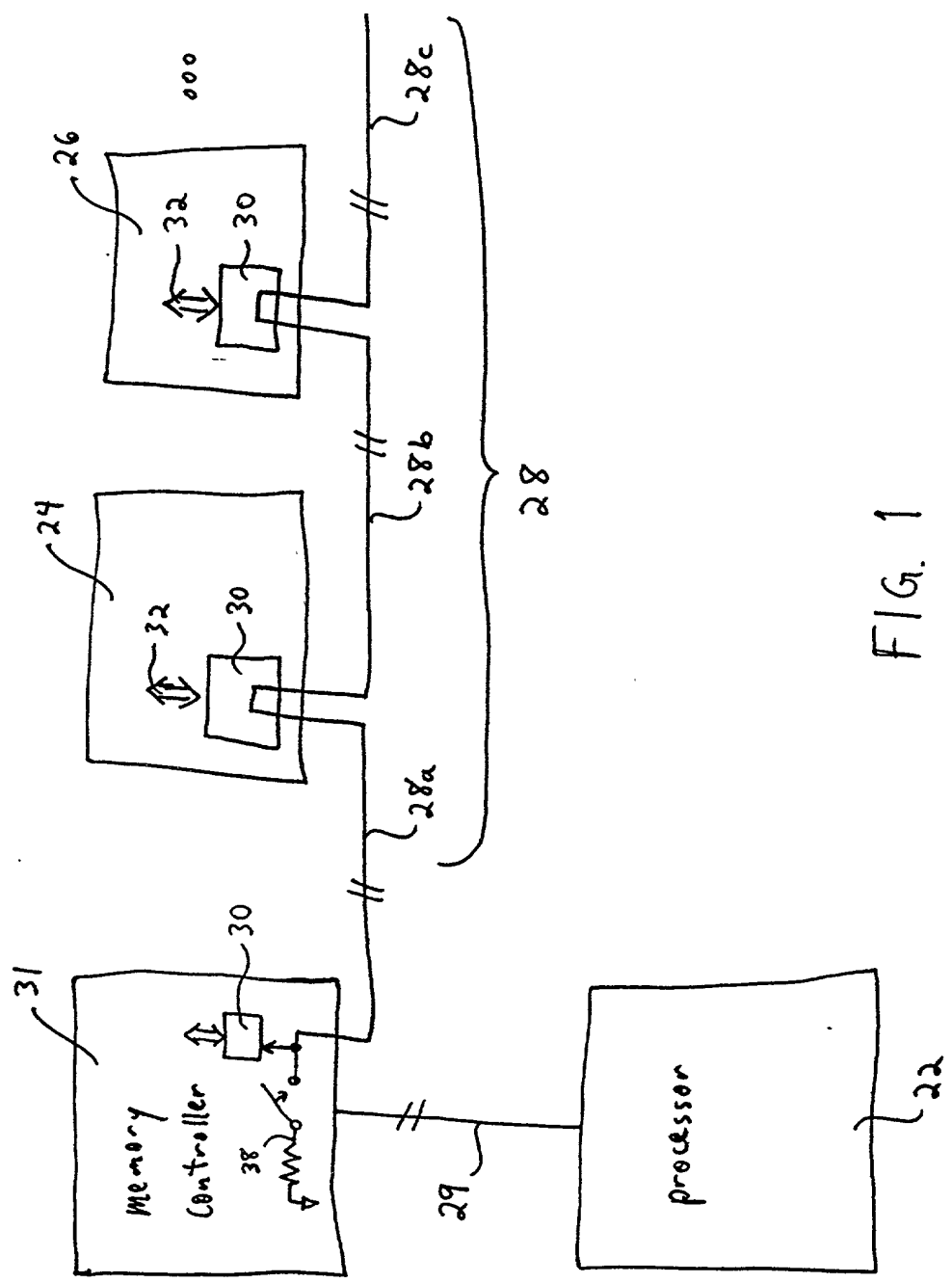


FIG. 1

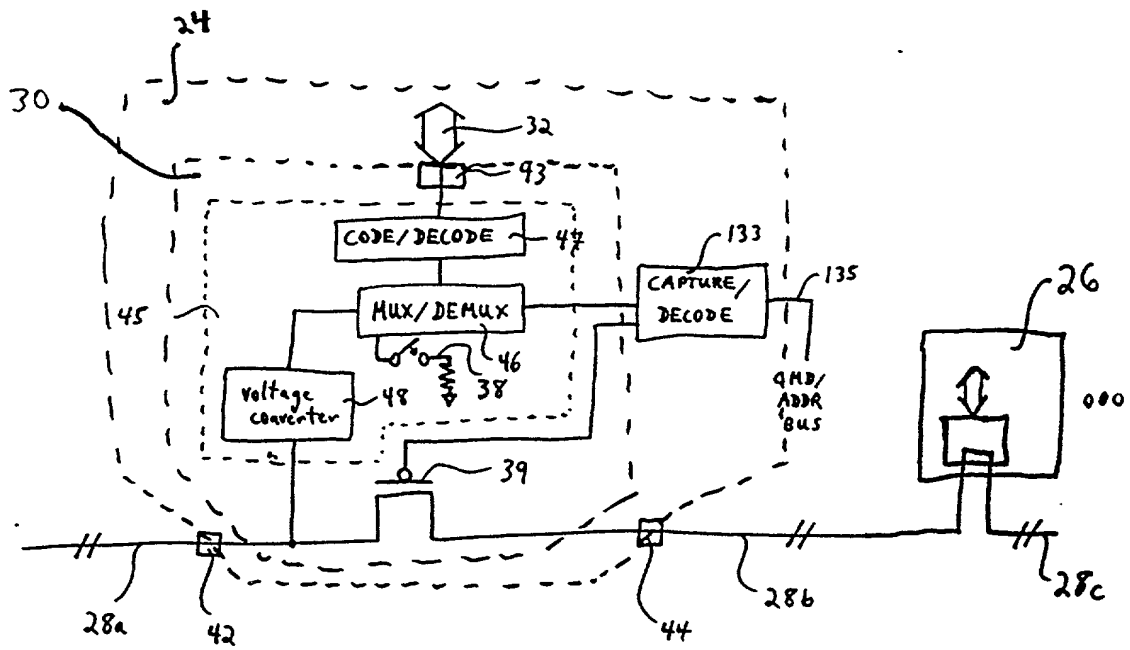


FIG. 2

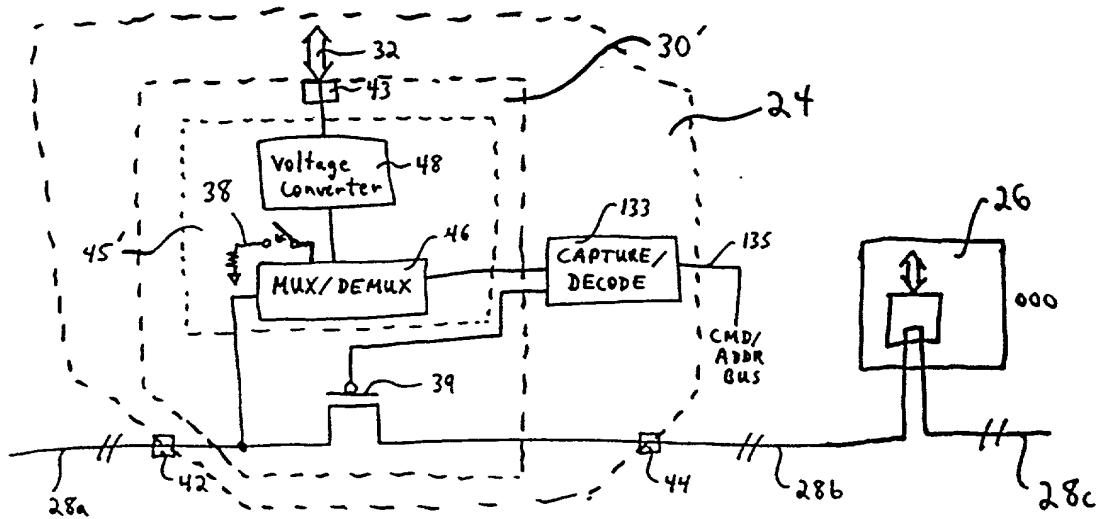


FIG. 3

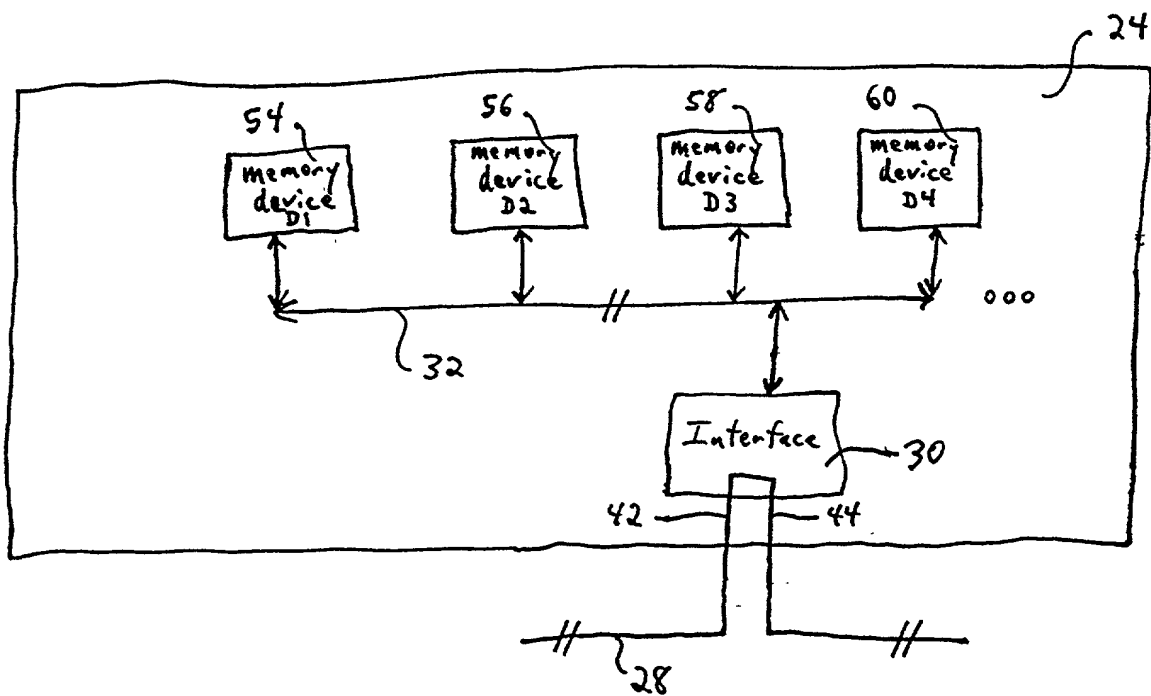


FIG. 4

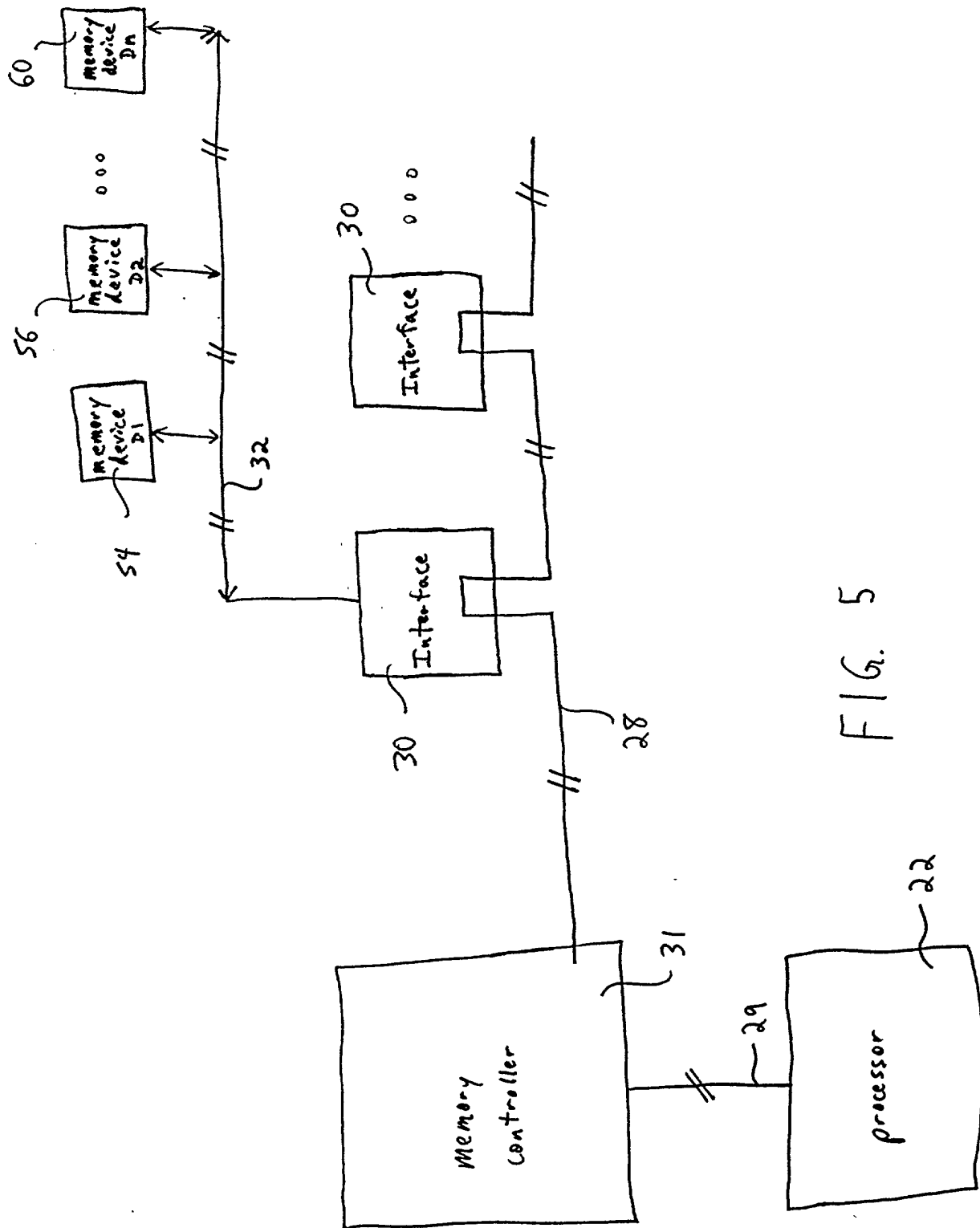


FIG. 5

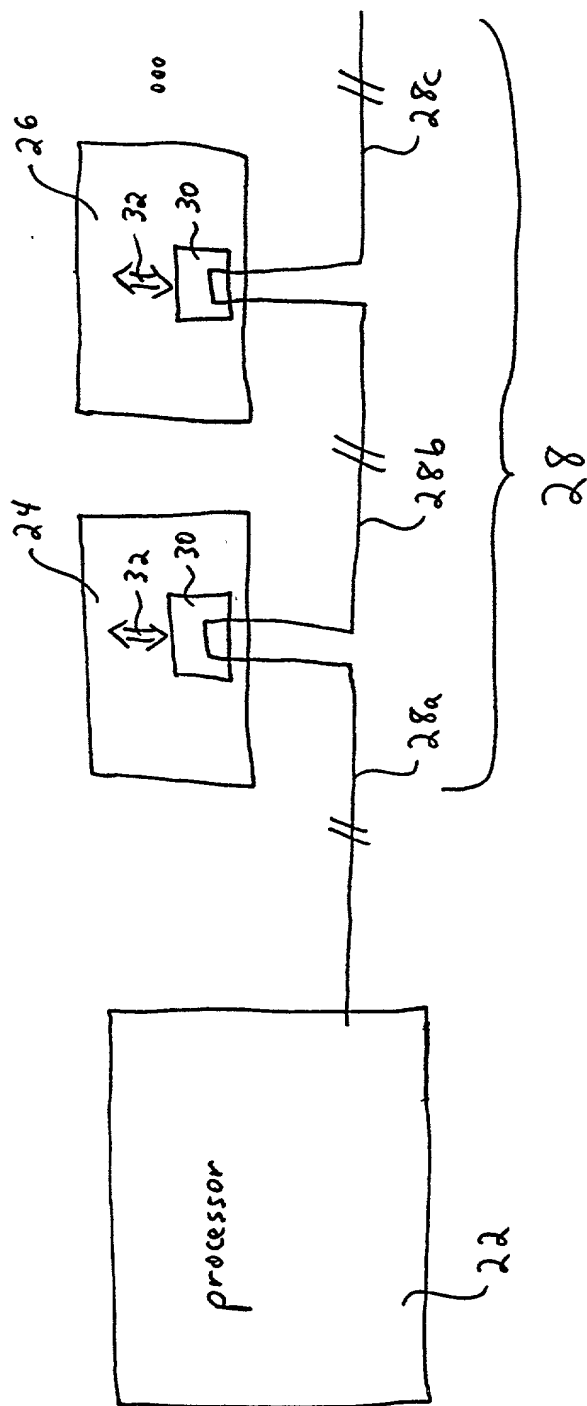


FIG. 6

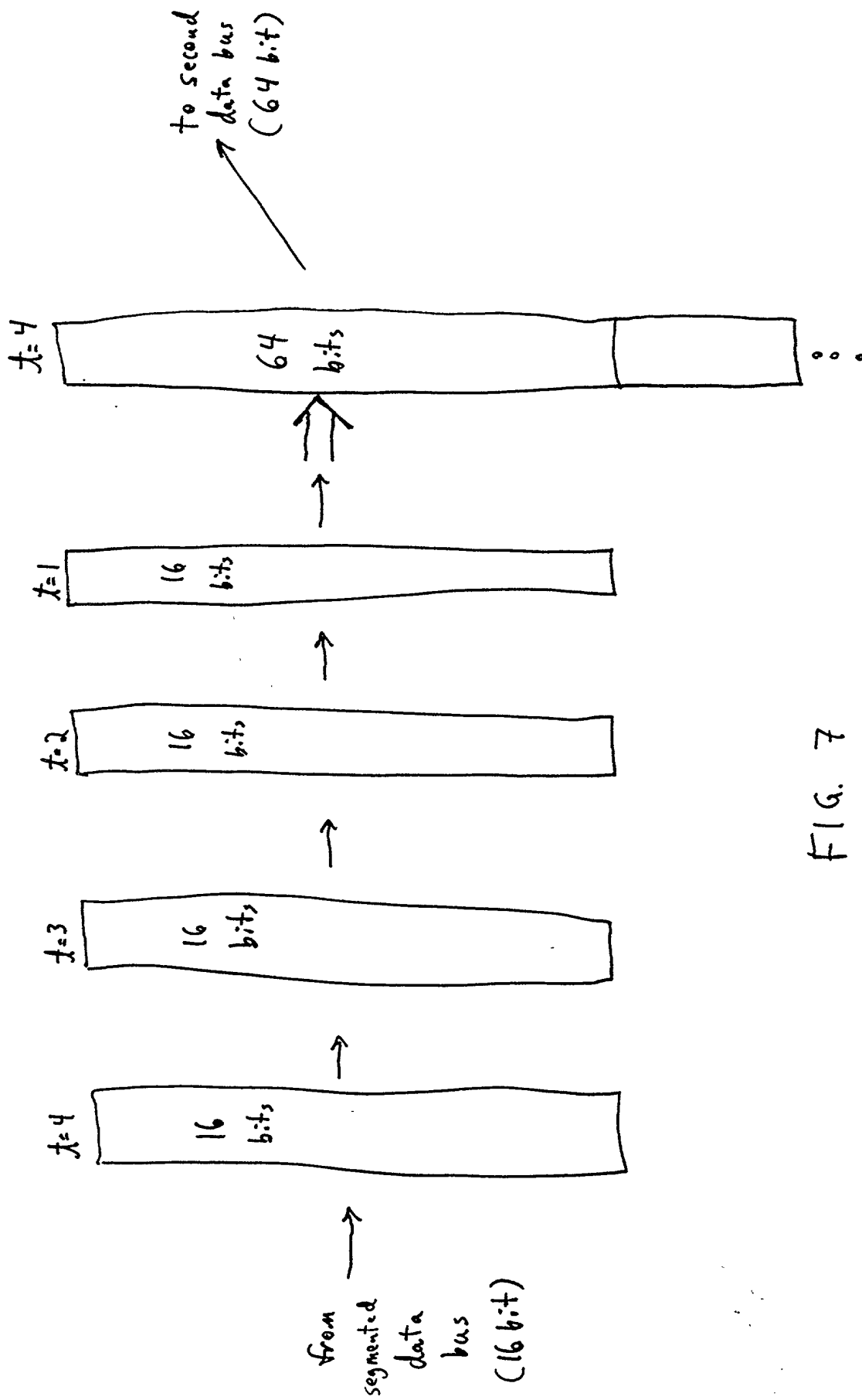


Fig. 7

FIG. 8 is a block diagram of a system 28 including a processor 22, a memory device 24, and a memory controller 26. The processor 22 is connected to the memory device 24 via a memory controller 26. The memory device 24 includes a memory array 30 and a memory controller 32. The memory controller 26 is connected to the memory array 30 via a memory controller 34. The memory controller 26 is also connected to a memory controller 36. The memory controller 36 is connected to a memory controller 38.

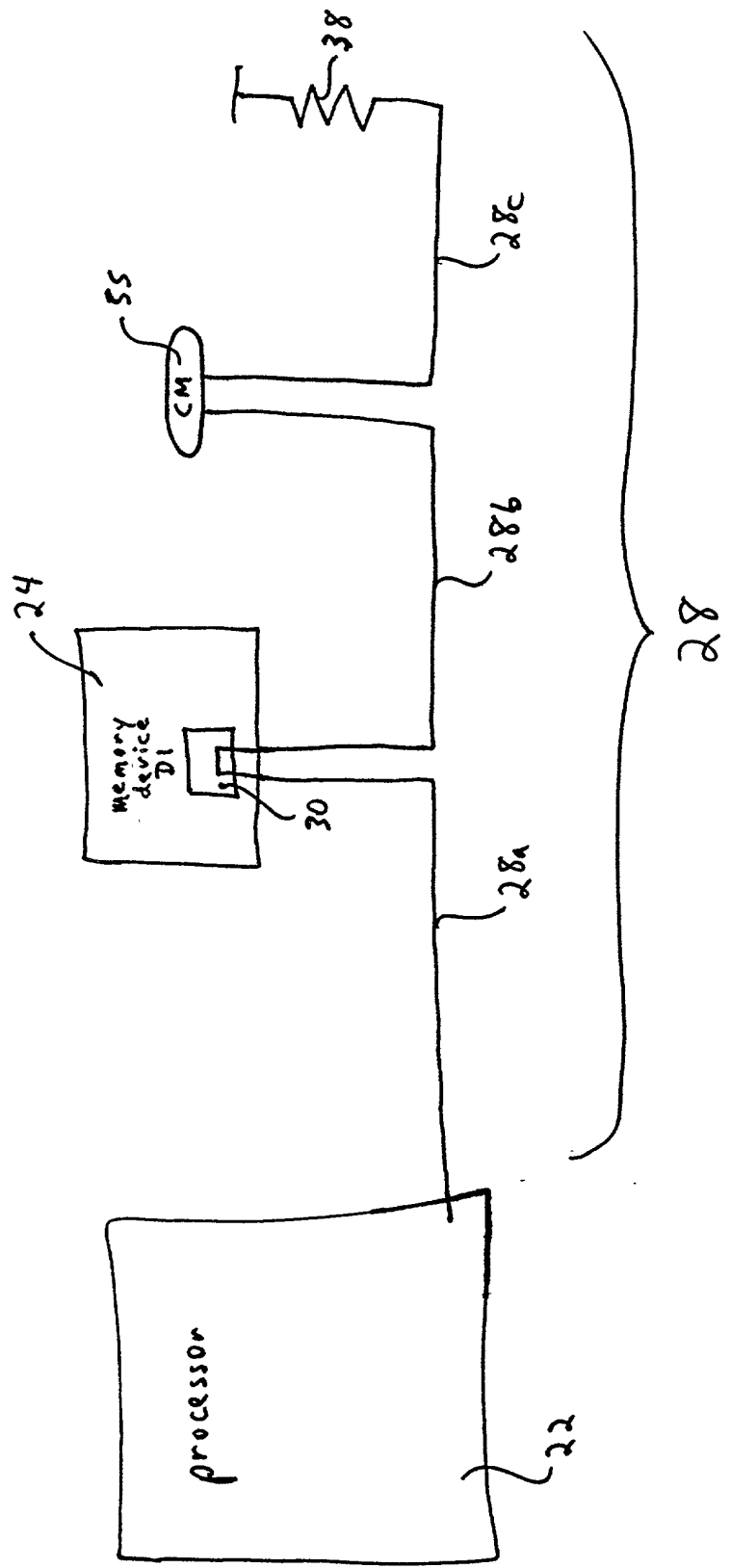
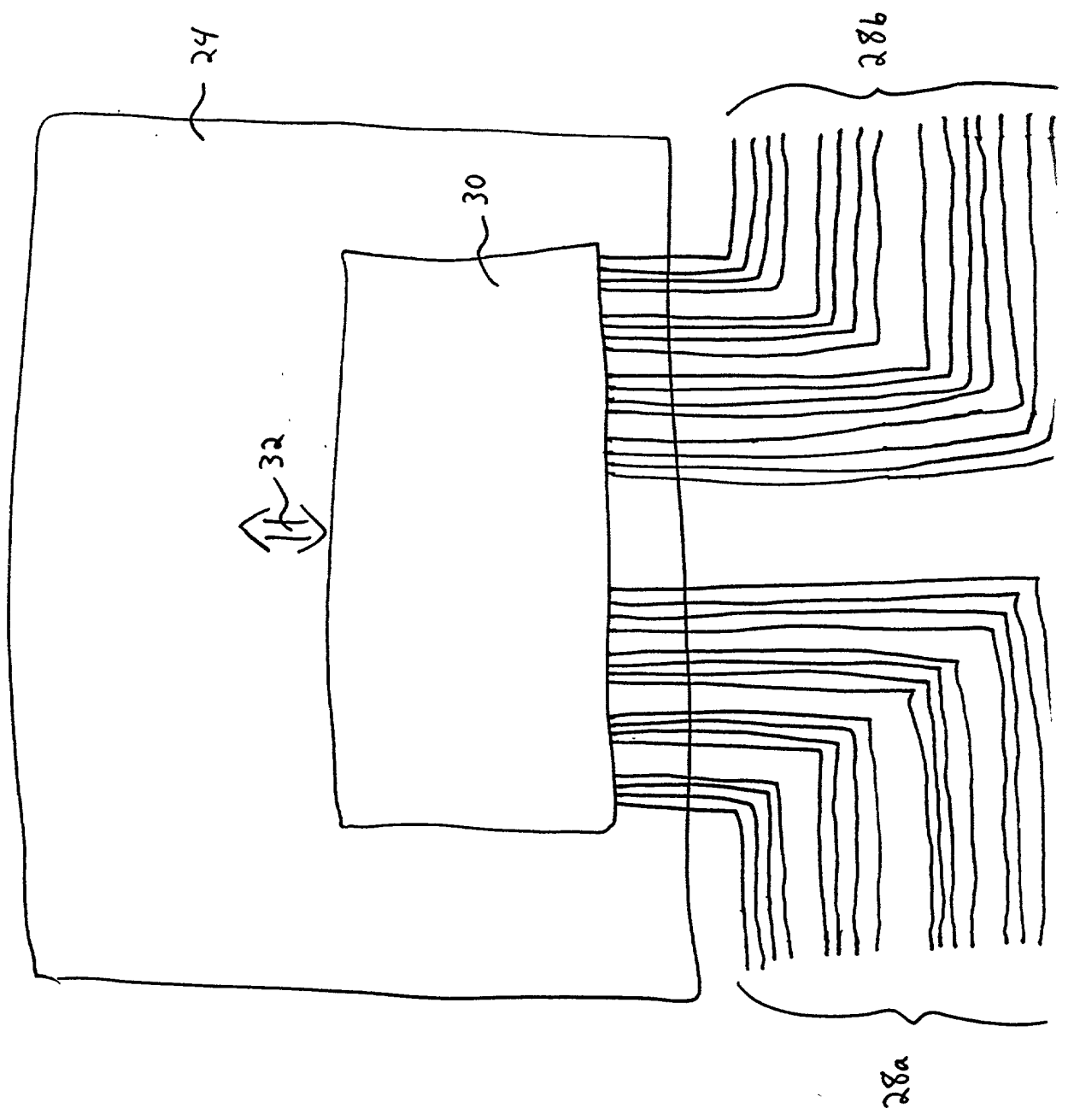


FIG. 8

FIG. 9





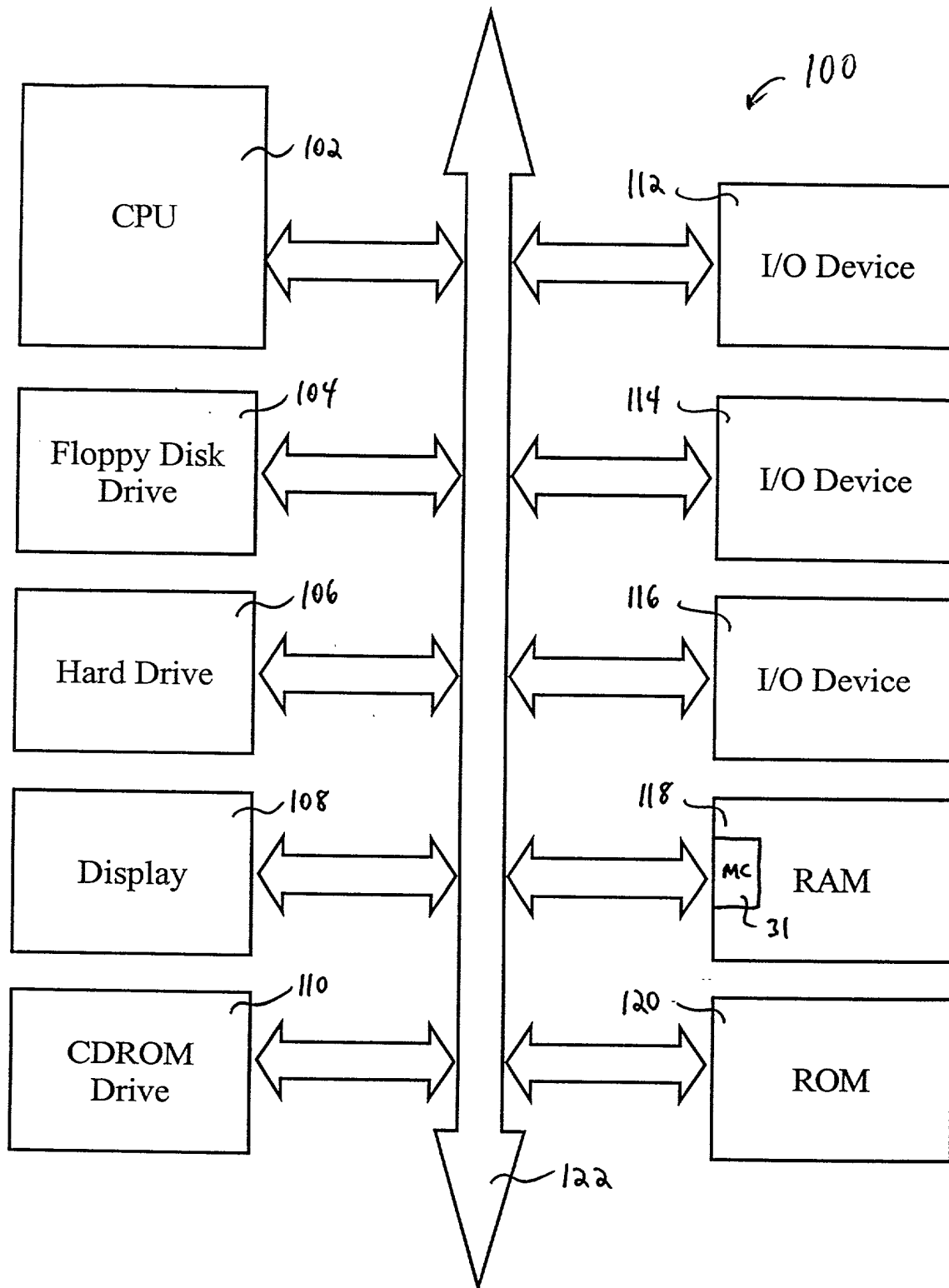


FIG. 10

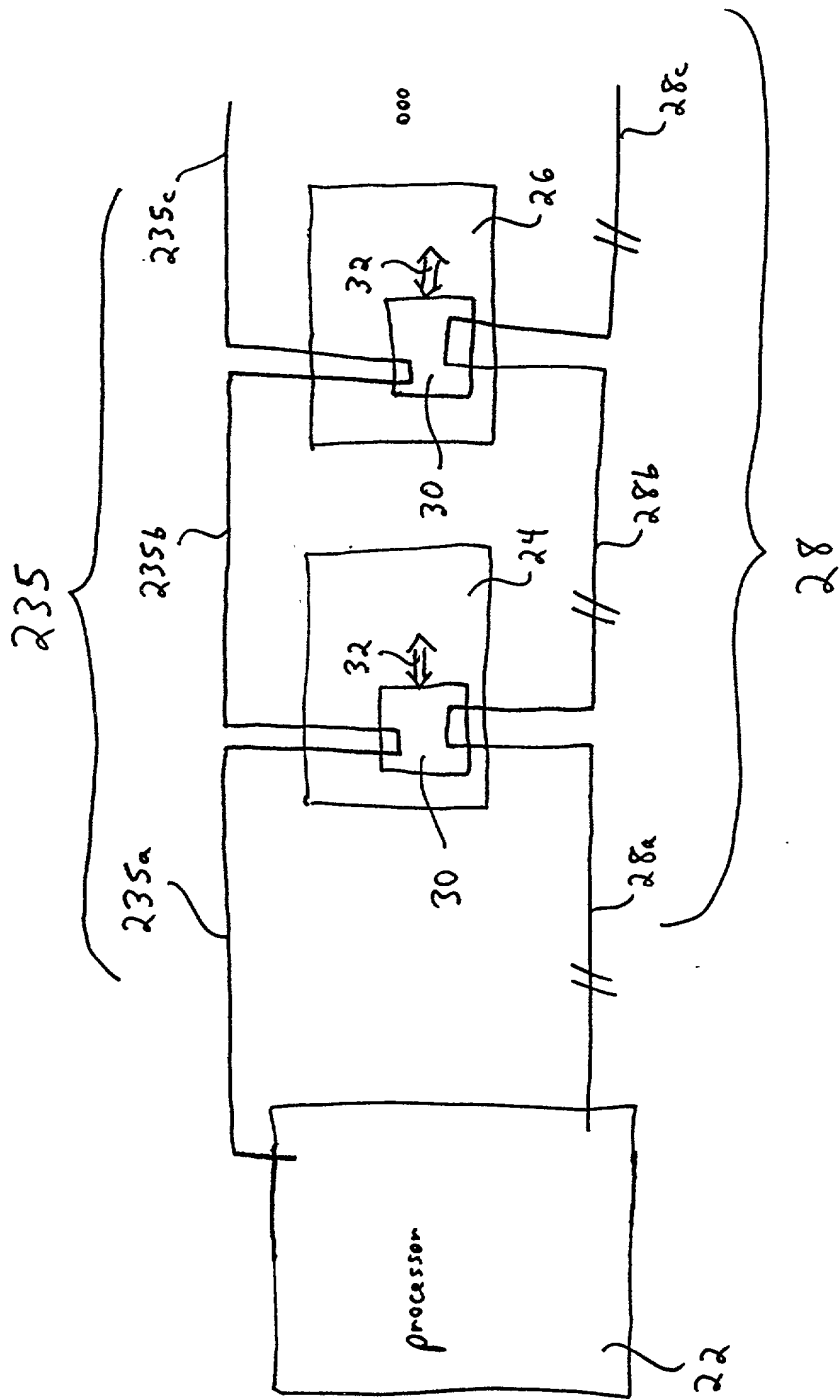


FIG. 11

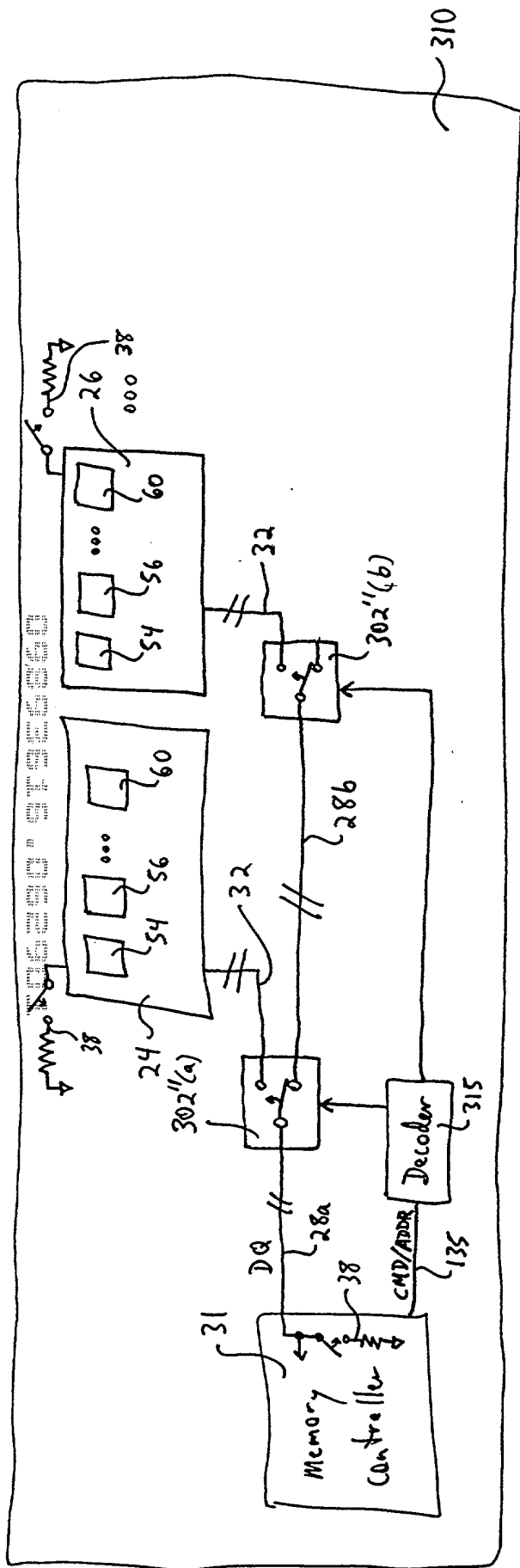


FIG. 12

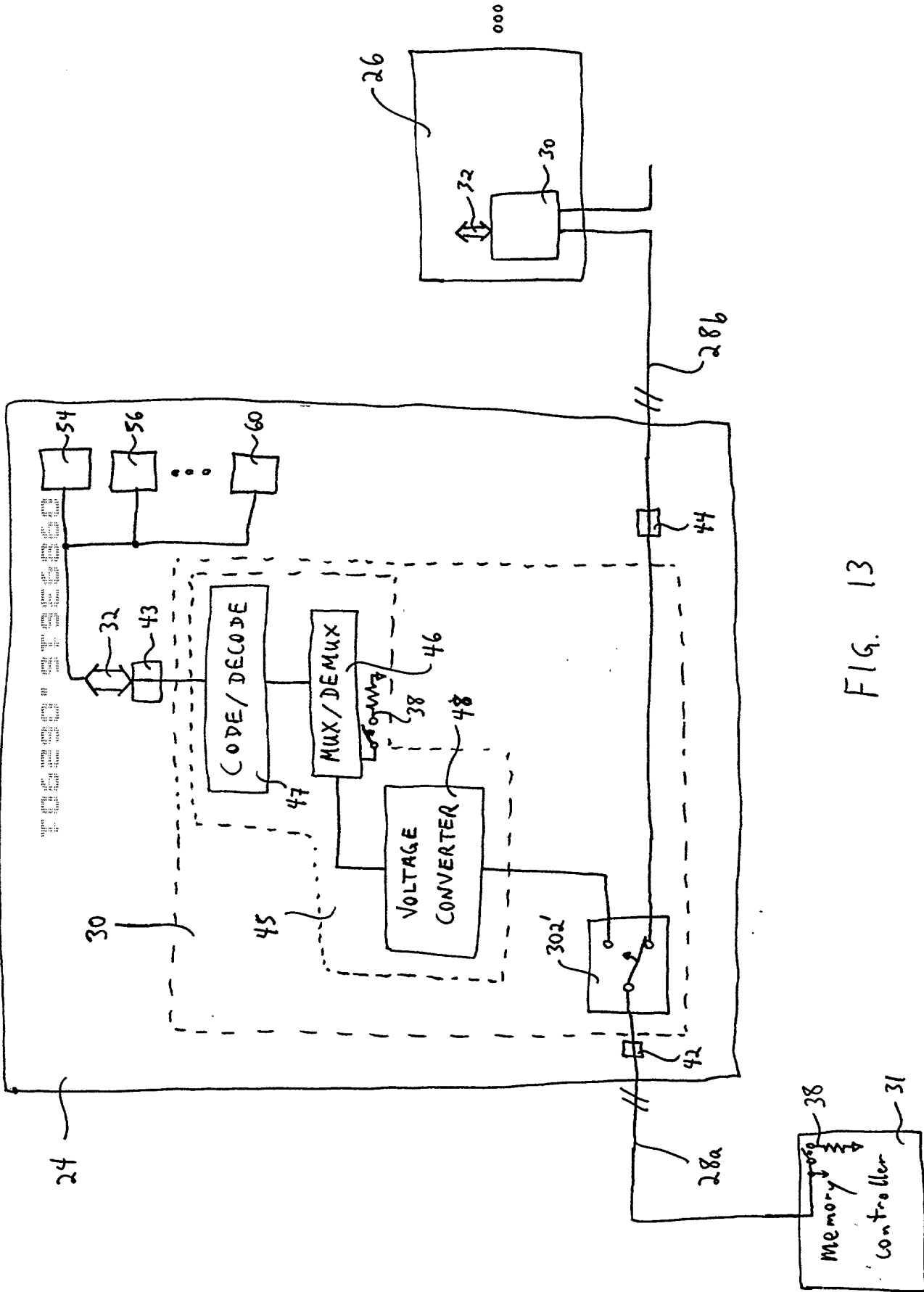


FIG. 13

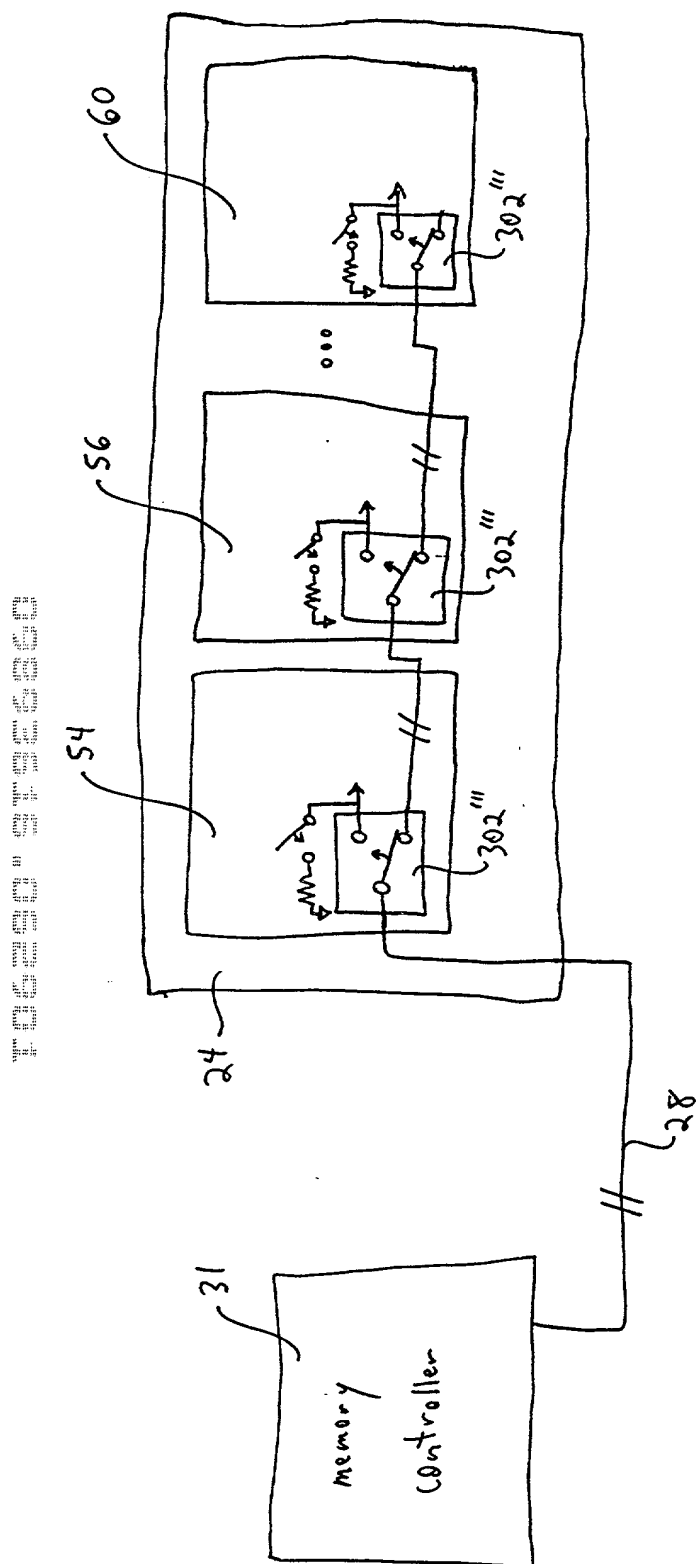


Fig. 14

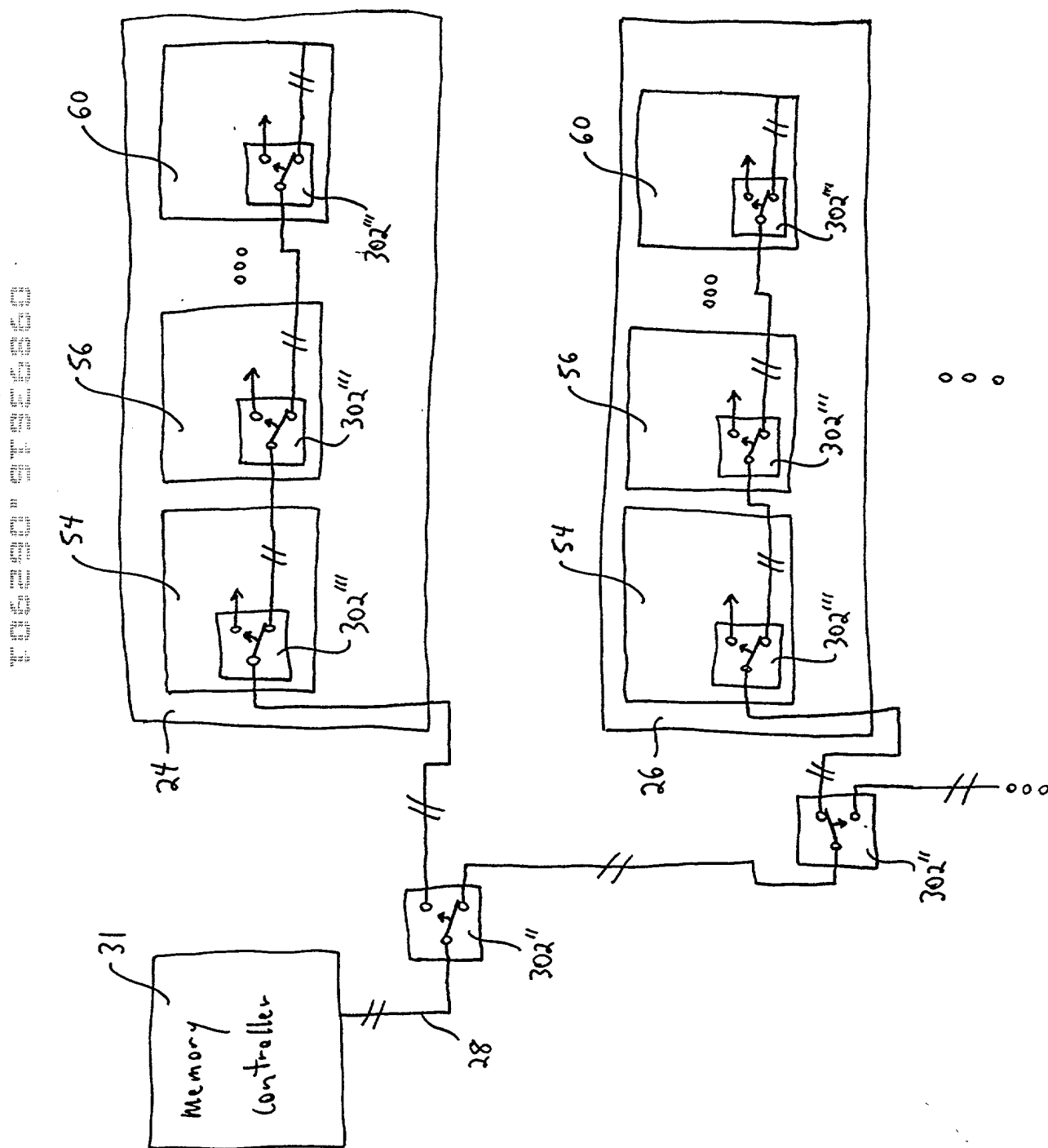


Fig. 15







A block diagram of a system. On the left, a large block labeled '31' contains a sub-block labeled 'Controller'. A horizontal line, labeled '28' at its left end, extends from the controller to the right. This line passes through two break symbols (//). After the second break, the line reaches a switch labeled '39'. The switch is connected to a vertical line that leads to a block labeled '24'. This block contains a sub-block labeled 'programmable terminator' with reference numeral '452'. The line continues to the right, passing through another break symbol (//). It then reaches a second switch labeled '39', which is connected to a vertical line leading to a second block labeled '26'. This block also contains a sub-block labeled 'programmable terminator' with reference numeral '452'. The line continues to the right, passing through a final break symbol (//) and ending at a reference numeral '000'. The entire diagram is labeled with '000' at the top right.

1